UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,520	01/12/2007	Peter A. Sandon	BUR920030107US1	2038

32074 7590 03/19/2010

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 321-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

NOTIFICATION DATE	DELIVERY MODE
03/19/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

EFIPLAW@US.IBM.COM

Office Action Summary	Application No.	Applicant(s)	
	10/595,520	SANDON ET AL.	
	Examiner	Art Unit	
	PAUL B. YANCHUS III	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 13-20* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yukinari et al., US Patent no. 6,466,073 [Yukinari].

Regarding claim 14, Yukinari discloses an apparatus for changing a clock frequency, comprising:

a phase-lock-loop circuit for providing a constant frequency signal in synchronism with a reference clock signal, wherein the constant frequency signal has a frequency f [PLL circuit inherently provides the constant frequency signal in synchronism with a reference signal, Figure 1 and column 6, lines 10-19];

a plurality of divider circuits receiving the constant frequency output signal from the phase-lock-loop circuit, each divider circuit providing an output signal having a frequency given by f/d_n and synchronous with the constant frequency signal of the phase-lock-loop circuit (20), wherein d_n is a divider value of an nth divider circuit [elements 21a-h in Figure 1 and column 6, lines 10-29]; and

a multiplexer for receiving the output signals from the plurality of divider circuits and for selecting, based on a frequency selection signal, the output signal from one of

the plurality of divider circuits, having a desired frequency, to serve as a processor clock signal [element 23 in Figure 1, column 1, lines 16-20 and column 6, lines 29-38].

Regarding claim 15, Yukinari discloses that the processor clock signal frequency may be changed according to the frequency selection signal [column 2, lines 29-38].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 5-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaushik et al., US Patent Application Publication no. 2005/0022038 [Kaushik], in view of Mirov et al., US Patent no. 6,728,890 [Mirov].

Regarding claim 1, Kaushik discloses a method for changing a clock frequency in a system comprising a plurality of synchronous integrated circuit chips, comprising:

detecting a change in processing requirements in one of the plurality of synchronous integrated circuit chips [utilization information and a determination of whether to increase or decrease frequency is detected for processors, paragraph 0009]; and

changing the clock frequency of the plurality of integrated circuit chips [frequency is changed to the desired frequency operating point of the highest utilization processor, paragraphs 0017-0019].

In summary, Kaushik discloses changing the operating frequency of a plurality of processors to the frequency desired by the processor with the highest utilization. Kaushik is silent as to how the clock frequency of the plurality of integrated circuit chips is changed. Mirov discloses a method of changing the clock frequency of a plurality of synchronous integrated circuit chips. Specifically, Mirov discloses that it is important to coordinate clock frequency changes among synchronous components to avoid corruption of signals traveling between the components [column 5, lines 54-67]. In order to accomplish this, Mirov discloses:

notifying the plurality of synchronous integrated circuit chips that a clock frequency change is to occur [new frequency values are written to registers of components and a Freeze signal is asserted, column 6, lines 61-67 and column 7, lines 51-63];

achieving a quiescent bus state in each of the plurality of synchronous integrated circuit chips [transactions between components are suspended, column 7, lines 64-67];

notifying the plurality of synchronous integrated circuit chips that the clock frequency change may occur [after all components have sent Freeze Acknowledge signals indicating that they suspended bus transactions, the frequency is changed, column 8, lines 7-29].

It would have been obvious to one of ordinary skill in the art to use the Mirov method of changing a frequency of synchronous processors to change the frequency of the synchronous processors in Kaushik in order to ensure that the processors stay synchronized during and after the frequency transition [column 5, lines 54-67].

Regarding claim 2, Kaushik further discloses that the processor clock frequencies are changed [paragraphs 0017-0019].

Regarding claim 5, Mirov further discloses that changing the processor frequency comprises determining a new clock frequency, selecting a divider value for adjusting an existing clock frequency, and applying the divider value to the existing clock frequency to obtain the new clock frequency [column 9, lines 58-65].

Regarding claim 6, Mirov discloses that notifying the plurality of synchronous integrated circuit chips that the clock frequency change may occur takes place only after all of the plurality of synchronous integrated circuit chips have achieved a quiescent bus state [after all components have sent Freeze Acknowledge signals indicating that they suspended bus transactions, the frequency is changed, column 8, lines 7-29].

Regarding claim 7, Kaushik, as described above, discloses a processor request to change clock frequency [utilization information and a determination of whether to increase or decrease frequency is detected for processors, paragraph 0009]. Mirov further discloses a companion chip that broadcasts the control transaction to the plurality of processors [new frequency values are written to registers of components and a power controller asserts a Freeze signal is asserted, column 6, lines 61-67 and column 7, lines 51-63]. Mirov further discloses that the functions of the companion chip may be executed by one of the plurality of processors [column 7, lines 10-14].

Regarding claim 8, Mirov further discloses that the companion chip broadcasts the control transaction over a bus that interconnects the companion chip and the plurality of processors, and that the plurality of processors obtain the control transaction

by snooping the bus [a power controller asserts a Freeze signal is asserted, Figure 2, column 6, lines 61-67 and column 7, lines 51-63].

Regarding claims 9 and 10, Mirov discloses that after being notified that a clock frequency change is to occur, each of the plurality of processors achieves a quiescent bus state and sends an acknowledgement to the companion chip and that the companion chip notifies the processors that the frequency change may occur after receiving all acknowledgements have been received [after all components have sent Freeze Acknowledge signals indicating that they suspended bus transactions, a Change signal is asserted, column 8, lines 7-29].

Regarding claim 11, Mirov discloses that the processors change frequencies [column 8, lines 21-24].

Regarding claim 13, Mirov further discloses that the function of the companion chip may be executed by one of the processors [column 7, lines 10-14].

Claims 3, 4, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaushik et al., US Patent Application Publication no. 2005/0022038 [Kaushik] and Mirov et al., US Patent no. 6,728,890 [Mirov], in view of Kahn, US Patent no. 7,290,161.

Kaushilk and Mirov, as described above, disclose achieving a quiescent bus state in each of the plurality of synchronous integrated circuit chips before changing the processor frequencies. Kaushik and Mirov are silent as to the how the processor bus frequencies are affected during the frequency change. Kahn discloses maintaining a

constant ratio between a processor frequency and a processor bus frequency in all operating modes [column 2, lines 49-54 and column 8, lines 34-39]. Therefore, both processor and bus frequencies are changed. Since both the processor and bus frequencies are changed, the bus clock would be stopped when the processor clock is stopped during the frequency change. It would have been obvious to one of ordinary skill in the art to maintain a constant ratio between the processor and bus clocks in Kaushik in order to allow both of the processor clock and bus frequencies to be set to lower frequencies and consequently reduce power consumption [Kahn, column 3, lines 18-27].

Claims 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yukinari et al., US Patent no. 6,466,073 [Yukinari][1], in view of Yatsuda et al, US Patent no. 6,845,462 [Yatsuda].

Regarding claim 16, Yukinari is silent as to how a bus frequency is generated for the processor. Yatsuda discloses generating a processor bus frequency by dividing the processor clock frequency [Figure 2 and column 4, lines 47-57]. It would have been obvious to one of ordinary skill in the art to use the Yatsuda method to generate a processor bus signal for the Yukinari processor.

Regarding claim 18, Yukinari is silent as to the structure of the PLL circuit. Yatsuda discloses a known PLL circuit that comprises a feedback divider and a reference clock signal that are input into the PLL [Figure 2 and column 4, lines 31-37].

[1] Cited in 4/25/06 IDS

It would have been obvious to one of ordinary skill in the art to use the known PLL circuit, as disclosed by Yatsuda, as the PLL circuit in Yukinari.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yukinari et al., US Patent no. 6,466,073 [Yukinari][2] and Yatsuda et al, US Patent no. 6,845,462 [Yatsuda], in view of Kahn, US Patent no. 7,290,161.

Yukinari and Yatsuda do not disclose that the frequency ratio of the processor clock and the bus clock is kept constant in all modes of operation. Kahn discloses maintaining a constant ratio between a processor frequency and a processor bus frequency in all operating modes [column 2, lines 49-54 and column 8, lines 34-39]. It would have been obvious to one of ordinary skill in the art to maintain a constant ratio between the processor and bus clocks in Yukinari and Yatsuda in order to allow both of the processor clock and bus frequencies to be set to lower frequencies in a low power mode and consequently reduce power consumption [Kahn, column 3, lines 18-27].

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

[2] Cited in 4/25/06 IDS

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Terrell, II, US Patent Application Publication no. 2004/0098631 discloses changing the operating frequency of a plurality of processors based on the utilization of the highest utilized processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL B. YANCHUS III whose telephone number is (571)272-3678. The examiner can normally be reached on Mon-Fri 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul B Yanchus/
Examiner, Art Unit 2116

March 13, 2010

/Thomas Lee/

Supervisory Patent Examiner, Art Unit 2115